GA20 / P32

Impact of Border Trap on mobility of Ge p-MOSFET with Al_2O_3/GeO_x/Ge gate stacks

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Abstract: *Interface traps (ITs) and border traps (BTs) in Al_2O_3/GeO_x/p-Ge gate stacks were characterized using deep-level transient spectroscopy (DLTS). Through evaluating the gate stacks with several thicknesses of GeO_x, the BTs in Al_2O_3, at Al_2O_3/GeO_x interface, in GeO_x were detected. The highest density of BT was found at Al_2O_3/GeO_x interface. Metal-oxide-semiconductor field-effect transistors (MOSFETs) with Al_2O_3/GeO_x/p-Ge gate stacks were evaluated and the impact of border trap on mobility are also discussed.*

Keywords: border trap, DLTS, Ge MOSFET

1. INTRODUCTION

Ge is one of the candidate materials for the future MOSFETs due to its high carrier mobility. For high mobility Ge MOSFET, stacked gate dielectric with thin Ge oxide interlayer, such as SiO_2/GeO_2 and Al_2O_3/GeO_x, has been studied actively [1,2]. On the other hand, in the case of Ge MOS, not only interface traps ITs but BTs located in gate dielectric are also problematic because it degrade MOS characteristics and mobility. For deep understanding and performance improvement of Ge MOS device, both the value and the position of BT in stacked gate dielectric should be clarified. However, in-depth study about BT in Ge stacked gate dielectric is limited [3]. Recently, we succeeded in separating the BT signal and IT signal using DLTS in SiO_2/GeO_2/Ge gate stacks grown by thermal and plasma oxidation [4]. In this study, we evaluated the density of IT (D_{it}) and density of BT (N_{bt}) in Al_2O_3/GeO_x/p-Ge gate stacks grown by post plasma oxidation (PPO). Additionally, we fabricated p-MOSFETs with Al_2O_3/GeO_x/p-Ge gate stacks and discussed the impact of BT on the devices.

2. EXPERIMENTAL

The fabrication process of MOS capacitors is as follows. P-type (100) Ge substrate with doping concentration of 2.3×10^{16} cm^{-3} was used. After chemical cleaning by acetone and HF solution, the first layer of Al_2O_3 was deposited at 300°C by atomic layer deposition (ALD) with trimethyl aluminum for 3, 9, 14 and 20 cycles, followed by PPO by electron cyclotron resonance (ECR). Then, the second layer of Al_2O_3 was deposited at 300°C by ALD for 25 cycles to suppress the current leakage. A 400°C post-deposition annealing (PDA) for 30 min was performed, TiN gate electrode was deposited by sputtering, followed by 350°C post-metallization annealing (PMA) for 20 min. After Al deposition, electrodes are patterned. Next, 300°C contact annealing (CA) for 10 min was carried out, and InGa back contact was formed. All the annealing in this study was performed in N_2 ambient.

Ge p-MOSFETs are fabricated on n-type (100) Ge substrate with doping concentration of 9.3×10^{15} cm^{-3}. After wafer cleaning, a SiO_2 field oxide for isolation was sputtered by ECR, and the active-area lithography was then carried out to define the active areas. To eliminate the damages resulting from sputtering and etching of the active area, sacrificial GeO_2 was formed by thermal oxidation at 450°C for 30 min in O_2 ambient and removed by rinse in a dilute HF solution. Next, an Al_2O_3/GeO_x/Ge gate stacked was fabricated by ALD and ECR method. After the 400°C PDA, the Al/TiN gate electrode was deposited and patterned. The BF_2 ion implantation was carried out with an acceleration energy of 30 keV and a dose of 10^{15} cm^{-2}. The Al/Pt source/drain contact was formed by lift-off method, followed by CA (for gate) and activation annealing (for source/drain) at 300°C for 10min in N_2 ambient. Subsequently, the InGa back contact was formed. P-MOSFET fabrication process and the device structure are shown in Figs. 1 (a) and (b), respectively. The implanted acceptor density of 4.3×10^{15} cm^{-3} was confirmed by Hall Effect measurement, and both D_{it} and N_{bt} were characterized using DLTS [4].

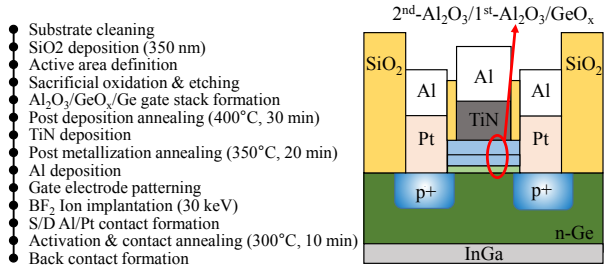

Fig. 1. Fabrication process and device structure of Ge p-MOSFETs with Al_2O_3/GeO_x gate stacks.

3. RESULTS AND DISCUSSION

3.1 Electrical properties of Ge MOS capacitors

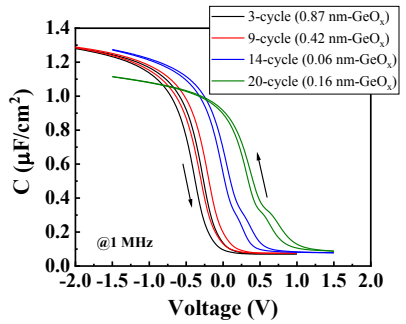

Fig. 2. *C-V* characteristics of Al/TiN/Al_2O_3/GeO_x/p-Ge MOS capacitors with different cycle number of 1st-Al_2O_3. The measurement was performed at RT and at a frequency of 1 MHz.

Table 1. Thickness information of Al/TiN/Al_2O_3/GeO_x/p-Ge MOS capacitors with different cycle number of 1st-Al_2O_3.

1st-Al_2O_3 cycle	1st-Al_2O_3 thickness (nm)	2nd-Al_2O_3 thickness (nm)	1st + 2nd Al_2O_3 EOT (nm)	MOS EOT (nm)	GeO_x EOT (nm) (MOS EOT-Al_2O_3 EOT)	GeO_x thickness (nm)
3-cycle	1.02	3.2	1.94	2.54	0.60	0.87
9-cycle	1.65	3.2	2.23	2.52	0.29	0.42
14-cycle	2.14	3.2	2.46	2.5	0.04	0.06
20-cycle	2.73	3.2	2.73	2.84	0.11	0.16

All samples showed typical *C-V* characteristics, as shown in Fig. 2. With increasing cycle number of the first layer of Al_2O_3, the flat band voltage (V_{FB}) shifts to the positive direction, and a bit stretch-out can be seen. The stretch-out in *C-V* may result from the thinner GeO_x. The thickness information including equivalent oxide thickness (EOT) for each oxide layer is shown in the Table 1.

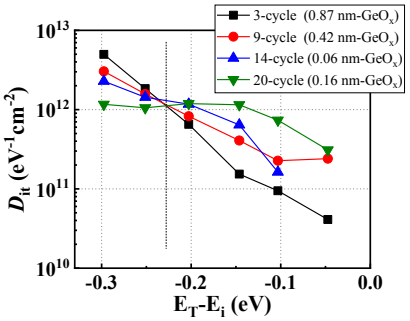

Fig. 3. Energy distribution of D_{it} for Al/TiN/Al_2O_3/GeO_x/p-Ge MOS capacitors with different cycle number of 1st-Al_2O_3.

Figure 3 shows the energy distribution of D_{it}. In the region close to mid-gap, the thicker GeO_x contributes to the lower D_{it}. This is reasonable and commonly accepted [1], and the tendency also well agrees with the *C-V* characteristics. However, in the region close to valence band, the thicker GeO_x shows higher D_{it}. The reason is unclear yet. One possibility is that the mechanism is similar to the effect of defect termination by Al atom after post-metallization annealing (Al-PMA), so the ITs close to valence b and are passivated [5].

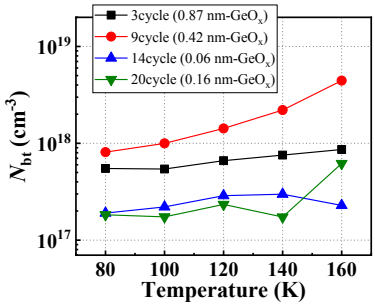

Fig. 4. Temperature dependence of N_{bt} for Al/TiN/Al_2O_3/GeO_x/p-Ge MOS capacitors with different cycle number of 1st-Al_2O_3.

Figure 4 shows the N_{bt} for all samples. Here, we measured BT which affect capture/emission of hole in valence band of Ge. With decreasing thickness of GeO_x, N_{bt} firstly increases and then decreases. The measured depth of BT is approximately 0.4 nm when the tunneling barrier height is the band offset of GeO_2 and Ge [4]. The locations of detected N_{bt} are demonstrated in Fig. 5. In the case of the thickest GeO_x (3 cycle-1st-Al_2O_3), BT in GeO_x is measured, as shown in Fig. 5(a). The value is comparable with our previous work about 1.8 nm-thick PPO GeO_2 [4]. In the case of 9 cycle-1st-Al_2O_3 corresponding 0.42 nm-thick GeO_x, BT located at the interface of Al_2O_3 and GeO_x is observed (Fig. 5(b)), and the value is the highest in this study. If the 1st-Al_2O_3 is thicker (14-20 cycle) corresponding thinner GeO_x, the measured BTs are located in the Al_2O_3 layer and N_{bt} is smaller than those of in GeO_x and Al_2O_3/GeO_x interface. Therefore, BT at Al_2O_3/GeO_x interface is the most serious for hole capture/emission in this stacked gate dielectric.

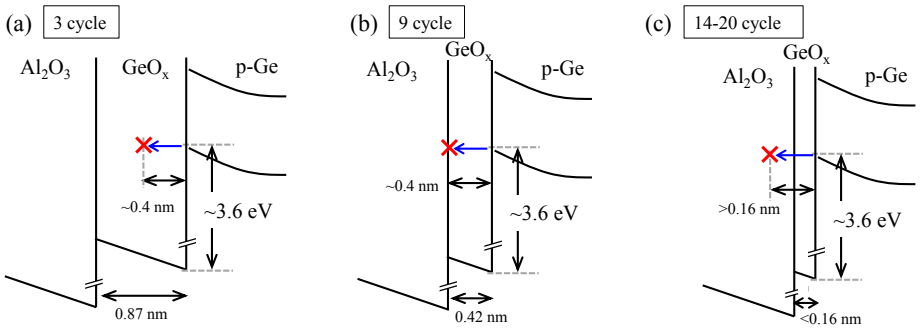

Fig. 5. Detected BT signals in band diagram of Al/TiN/Al_2O_3/GeO_x/p-Ge MOS capacitors with 1st-Al_2O_3 deposition for (a) 3 cycle, (b) 9 cycle and (c) 14-22 cycle.

3.2 Device performance of Ge p-MOSFETs

Figure 6 shows drain current (I_D) versus drain voltage (V_D) characteristics of pMOSFETs with the Al_2O_3/GeO_x/Ge gate stack. Here, the channel length (*L*) and width (*W*) are 120 and 390 m, respectively. The pMOSFET with higher cycle number of Al_2O_3 first layer showed the higher current drivability. Figure 7 shows source current (I_S) versus gate voltage (V_G) characteristics with V_D=-10mV. The threshold voltage (V_{TH}) was obtain from the x-axis interception of $I_S/g_m^{1/2}$ versus V_G plot, where is transconductance. With increasing cycle number of the first layer of Al_2O_3, the

V_{TH} shifts to the positive direction, which coincide with V_{FB} shift found in *C-V* characteristics of MOS capacitors. The effective mobility (μ) was calculated using I_S-V_G data with V_D=-10 mV and a formula of $\mu=g_m/[(W/L)C_{OX}V_D]$, where C_{OX} is an inversion channel capacitance experimentally obtained from the gate-channel capacitance.

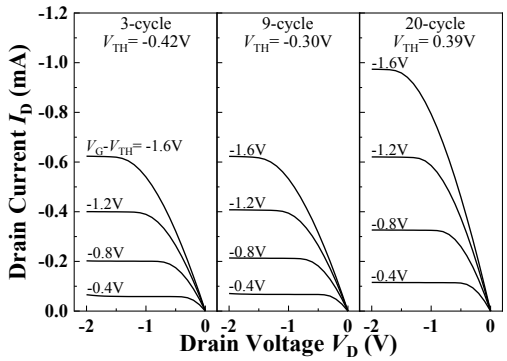

Fig. 6. I_D-V_D characteristics of Ge p-MOSFET with different cycle number of 1st-Al_2O_3. All the devices have Al_2O_3/GeO_x/Ge gate stacks. The *L* and *W* were 120 and 390 m, respectively.

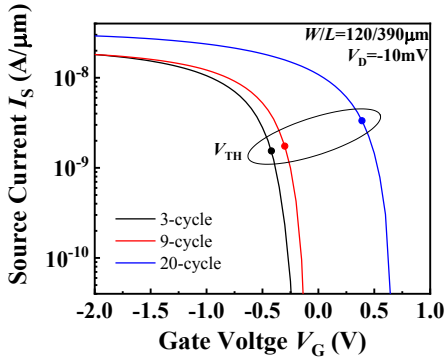

Fig. 7. I_S-V_G characteristics of Ge p-MOSFET with different cycle number of 1st-Al_2O_3.

Figure 8 shows the effective mobility as a function of inversion carrier density. The highest peak mobility was obtained from the MOSFET with 20-cycle-1st-Al_2O_3 even in the high-field region. A delay of signal rising can be seen in this device, which may result from the Coulomb scattering of ITs. MOSFET with 9-cycle-1st-Al_2O_3 showed the lowest mobility among all devices, and the mobility value of the MOSFET with 3-cycle-1st-Al_2O_3 are in between. In the low-field region, degradation of mobility is generally considered as an effect of surface roughness due to the channel carrier gathering near the surface under high electric field. However, the wafer condition and the fabrication process of these devices are the same, and we believed there should be no discrepancy in the roughness. Instead of surface roughness, here we considered the effect of bolder trap as the main factor of mobility degradation in high-field region.

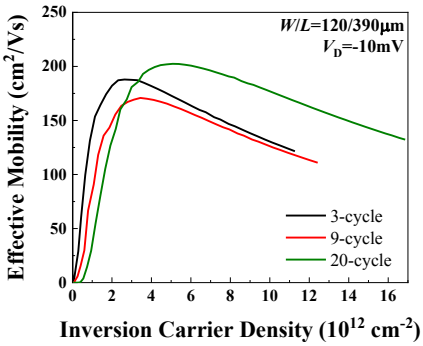

Fig. 8. Effective hole mobility in Ge p-NOSFET with different cycle number of 1st-Al_2O_3.

Figure 9 shows band diagrams of MOSFETs at different bias conditions. When the surface potential (Φ_S) equals to difference of Fermi level (E_F) and intrinsic Fermi level (E_i) (Ψ_B), corresponding to weak inversion, the ITs near mid gap are filled, thus showing negative charge, as shown in Fig. 9 (a). When Φ_S equals to Ψ_B + 0.23 eV, corresponding to the crossing point in Fig. 3, the IT charge become neutral and some carrier may be captured by BTs, as shown in Fig. 9 (b). When Φ_S is over Ψ_B + 0.5 band gap (E_g), corresponding to the high-field region (Fig. 9 (c)), even the donor-like ITs near valence band are filled with holes, the IT charge shows positive. Besides, a lot of holes are captured by the BTs in oxide layers. Since the capture cross section of BTs is very small, the capture may last for whole measurement. As a result, the high-field region, more carriers (holes) were captured by the BT in the oxide layer, thus degrading the mobility. According to the result of N_{bt}, the net effect of BT was less severe for the device with 20-cycle-1st-Al_2O_3, so the mobility reach a higher level than other conditions.

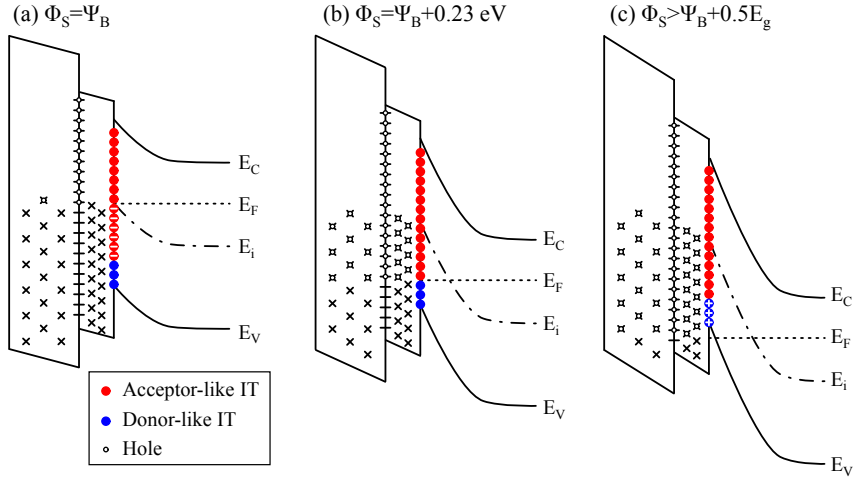

Fig. 9. Band diagrams of Ge p-MOSFET showing the occupancy of IT and BT when (a) Φ_S=Ψ_B, (b) Φ_S=Ψ_B+0.23 eV and (c) Φ_S>Ψ_B+0.5E_g (corresponding to high field region). IT charges are negative at condition (a), neutral at condition (b) and negative at condition (c).

4. CONCLUSION

We evaluated D_{it} and N_{bt} of Al_2O_3/GeO_x/p-Ge gate stacks with different GeO_x thickness by using DLTS. By changing GeO_x thickness, we can separately evaluate N_{bt} in GeO_x, N_{bt} at Al_2O_3/GeO_x interface, and N_{bt} in Al_2O_3. The D_{it} near to mid-gap is lower in the thicker GeO_x. By contrast, the D_{it} near to the valence band is lower in the thinner GeO_x. BTs are mainly located at the interface of Al_2O_3 and GeO_x. Surface roughness may not be the only factor of mobility degradation in high-field region. The BTs in oxide layers play an important role as well. Therefore, good quality oxide layers and adequately high band offset of oxide layers are important for high performance MOSFETs.

5. REFERENCES

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